What is Claimed is:

1. A synchronization system for synchronizing period signals generated by a plurality of systems composing a synchronous-multisystem apparatus wherein any particular one of said systems comprises:

a synchronization-reference selecting circuit for selecting a period signal generated by one of said systems by referring to a period signal generated by said particular system and period signals generated by said systems other than said particular system and outputting a signal of a period corresponding to said selected period signal as a synchronization-reference signal; and

a control-period correcting circuit for correcting a period of a period signal generated by said particular system on the basis of a synchronization shift between said period signal generated by said particular system and said synchronization-reference signal;

wherein:

if said synchronization-reference signal is output by said synchronization-reference selecting circuit, said control-period correcting circuit forms a judgment on said synchronization shift between said period signal generated by said particular system and said synchronization-reference signal and corrects said period of said period

signal generated by said particular system on the basis of a result of said judgment; and

if said synchronization-reference signal is not output by said synchronization-reference selecting circuit, on the other hand, said control-period correcting circuit does not correct said period of said period signal generated by said particular system.

2. A synchronization system according to claim 1 wherein:

said synchronization-reference selecting circuit has a judgment circuit for forming a judgment as to whether or not the number of signals consisting of a period signal generated by said particular system and period signals generated by said systems other than said particular system output during a synchronization-reference selection period with a length equal to that of a control period of said particular system including a start point of said period signal of said particular system has attained a majority of said period signals generated by all said systems; and

if said judgment circuit determines that said majority has been attained, said synchronization-reference signal is output.

3. A synchronization system according to claim 2 wherein said synchronization-reference selection period starts at a point of time leading ahead of said start point

of a period signal of said particular system by a half of said control period and ends at a point of time lagging behind an outputting time of said period signal of said particular system by a half of said control period.

4. A synchronization system according to any one of claims 1 to 3 wherein:

if said synchronization-reference signal is not output during a synchronization-reference selection period with a length equal to that of a control period of said particular system including a start point of said period signal of said particular system, said control-period correcting circuit does not correct a period of a period signal generated by said particular system; and

if said synchronization-reference signal is output during said synchronization-reference selection period, on the other hand, said control-period correcting circuit corrects said period of said period signal generated by said particular system in accordance with whether said period signal generated by said particular system leads ahead of or lags behind said synchronization-reference signal.

5. A synchronization system according to claim 4 wherein, with said synchronization-reference signal output during said synchronization-reference selection period, said control-period correcting circuit:

shortens a period of a period signal generated by said particular system if said synchronization-reference signal is output, leading ahead of said period signal generated by said particular system; or

lengthens said period of said period signal generated by said particular system if said synchronization-reference signal is output, lagging behind said period signal generated by said particular system.

6. A synchronization system according to any one of claims 1 to 3 wherein said control-period correcting circuit:

shortens a control period of a period signal generated by said particular system by a predetermined amount of time if said synchronization-reference signal is output during a period of time between a particular point of time said period signal is generated by said particular system and an earlier point of time leading ahead of said particular point of time by a half of said control period;

lengthens said control period by a predetermined amount of time if said synchronization-reference signal is output during a period of time between said particular point of time and a later point of time lagging behind said particular point of time by a half of said control period;

does not correct said control period if said synchronization-reference signal is output at said

particular point of time; or

does not correct said control period if said synchronization-reference signal is not output during a period of time between said earlier point of time and said later point of time.

7. A synchronization system according to any one of claim 2 or 3 wherein:

said synchronization-reference selecting circuit further has a period-signal-validity setting circuit provided for each of period signals generated by said particular system as well as said systems other than said particular system and used for determining whether each of said period signals is valid or invalid; and

said judgment circuit forms a judgment as to whether or not the number of period signals which are judged to be valid by said period-signal-validity setting circuit and output during a synchronization-reference selection period has attained a majority of said valid period signals.

8. A synchronization system according to any one of claim 2 or 3 wherein:

said synchronization-reference selecting circuit has a counter circuit provided for each of said systems and used for counting the number of times said particular system and said systems do not output period signals during a period of time between an early point of time leading

ahead of a particular point of time a period signal is generated by said particular system by a half of a control period and a later point of time lagging behind said particular point of time by a half of said control period; and

when a count value of said counter circuit reaches a value determined in advance, said judgment circuit forms a judgment as to whether or not the number of period signals excluding period signals associated with said counter circuit has reached a majority of said period signals excluding period signals associated with said counter circuit.

9. A synchronization system according to claim 4 wherein:

said control-period correcting circuit further has a storage circuit for storing a period of time between a particular point of time said particular system outputs a period signal and a reference point of time said synchronization-reference signal is output;

if said synchronization-reference signal is generated within said synchronization-reference selection period, leading ahead of a period signal generated by said particular system, said period of time stored in said storage circuit is used as a next period of said period signal; and

if said synchronization-reference signal is generated within said synchronization-reference selection period, lagging behind a period signal generated by said particular system, on the other hand, said period signal generated by said particular system is judged to be a leading period signal and, in this case, a value obtained as a result of addition of said period of time stored in said storage circuit to a predetermined period of time is used as a next period of said period signal.

10. A synchronization system according to claim 9 wherein:

said control-period correcting circuit reads out said period of time stored in said storage circuit each time a period signal is output; and

if said period of time stored in said storage circuit is within a predetermined range, a synchronization abnormality is judged to have occurred in said particular system.

11. A synchronization system according to claim 10 wherein, if a synchronization abnormality is judged to have occurred in said particular system, a period signal generated by said particular system is synchronized by said control-period correcting circuit to a period signal generated by one of said systems other than said particular system.

12. A synchronization system according to claim 1, wherein:

said synchronization-reference selecting circuit further has a period-signal-validity setting circuit provided for each of period signals generated by said particular system as well as said systems other than said particular system and used for determining whether each of said period signals is valid or invalid;

said judgment circuit forms a judgment as to whether or not the number of period signals which are judged to be valid by said period-signal-validity setting circuit and output during a synchronization-reference selection period has attained a majority of said valid period signals; and

if a synchronization abnormality is judged to have occurred in said particular system, said control-period correcting circuit in each of said systems gives a command to temporarily set a period signal generated by said particular system as a valid period signal to said period-signal-validity setting circuit.

13. A synchronization system according to any one of claims 4 to 6 wherein:

each of said systems has a period-signal generating circuit provided with a timer circuit allowing a restart time to be set therein at a value expressed in terms of clock-cycle units;

when a time indicated by said timer circuit matches a period of a period signal, said period-signal generating circuit outputs a period signal and restarts said timer circuit;

if a period signal generated by said particular system is synchronized with said synchronization-reference signal, said restart time of said timer circuit is set by said control-period correcting circuit at a value of 1;

if a period signal generated by said particular system lags behind said synchronization-reference signal, said restart time of said timer circuit is set by said control-period correcting circuit at a value of 2; and

if a period signal generated by said particular system leads ahead of said synchronization-reference signal, said restart time of said timer circuit is set by said control-period correcting circuit at a value of 0.

14. A synchronization system according to claim 1 wherein:

each of the same plurality of systems further has a communication circuit for exchanging information on synchronization among said systems and a delay circuit for delaying a period signal;

when a period signal is generated by said particular system, said communication circuit of said particular system transmits information on synchronization to said

systems other than said particular system, receives information on synchronization from said systems other than said particular system and finds a length of a transmission time it takes to transmit information on synchronization; and

said delay circuit delays a period signal by said length of said transmission time found by said communication circuit.

15. A synchronous-multisystem control apparatus comprising a plurality of systems each for generating a period signal wherein:

any particular one of said systems starts processing at a point of time a period signal is generated by said particular system; and

a peripheral unit synchronizes period signals generated by said systems with each other by adopting a synchronization system according to any one of claims 1 to 14.

16. A synchronization system for synchronizing period signals generated by a plurality of systems composing a synchronous-multisystem apparatus wherein any particular one of said systems comprises:

a synchronization-reference selecting means for selecting a period signal generated by one of said systems by referring to a period signal generated by said

particular system and period signals generated by said systems other than said particular system and outputting a signal of a period corresponding to said selected period signal as a synchronization-reference signal; and

a control-period correcting means for correcting a period of a period signal generated by said particular system on the basis of a synchronization shift between said period signal generated by said particular system and said synchronization-reference signal;

wherein:

if said synchronization-reference signal is output by said synchronization-reference selecting means, said control-period correcting means forms a judgment on said synchronization shift between said period signal generated by said particular system and said synchronization-reference signal and corrects said period of said period signal generated by said particular system on the basis of a result of said judgment; and

if said synchronization-reference signal is not output by said synchronization-reference selecting means, on the other hand, said control-period correcting means does not correct said period of said period signal generated by said particular system.

17. A synchronization method for synchronizing period signals generated by a plurality of systems

composing a synchronous-multisystem apparatus wherein any particular one of said systems executes the steps of:

selecting a period signal generated by one of said systems by referring to period signals generated by said systems and outputting a signal of a period corresponding to said selected period signal as a synchronization-reference signal provided that a majority of period signals have been generated by said systems during a predetermined synchronization-reference selection period;

correcting a period of a period signal generated by said particular system on the basis of a synchronization shift between said period signal generated by said particular system and said synchronization-reference signal wherein:

if said synchronization-reference signal is not output, a period of a period signal generated by said particular system is used as a period of said period signal; and

if said synchronization-reference signal is output, on the other hand, a period of a period signal generated by said particular system is shortened provided that said synchronization-reference signal is output, leading ahead of said period signal generated by said particular system, or said period of said period signal generated by said particular system is lengthened provided

that said synchronization-reference signal is output, lagging behind said period signal generated by said particular system.

18. A communication control apparatus for exchanging information in a packet format, said apparatus comprising:

a transmission control unit having a repeated-transmission function for consecutively transmitting a plurality of packets each including the same user information, a sequence number of transmission in which said packet is transmitted and a frame check sequence for examination of an error; and

a reception control unit having a frame-check-sequence examining means for detecting an error, a packet-identity judging means and a reception-history control means provided with a reception-count counter for counting the number of times said packets have been received so far, that is, substantially for detecting said sequence number of transmission of a packet currently being received,

wherein said reception control unit carries out reception processing only if at least one of said packets transmitted consecutively is received successfully and information on an error is recorded only if all said packets transmitted consecutively are received unsuccessfully.

19. A communication control apparatus according to

claim 18 wherein:

said information on an error includes information indicating a type of said error; and

said reception-history control means has an error-information generating means for selecting and outputting information on an error in accordance with a priority order set in advance in case errors with types different from packet to packet are detected during reception of packets transmitted consecutively.

20. A communication control apparatus according to claim 18 wherein:

said transmission control unit adds information indicating a type of a packet to be transmitted to said packet; and

only when said reception-history control means detects a last one of packets with the same type transmitted consecutively does said reception control unit carry out reception processing.

21. A communication control apparatus according to claim 18 wherein said reception-history control means sets said sequence number of transmission included in a received packet into said reception-count counter if no error is detected in said received packet.

22. A communication control apparatus according to claim 18 wherein said reception-history control means

increments a count value of said reception-count counter if an error is detected in a received packet by said frame-check-sequence examining means.

23. A communication control apparatus according to claim 18 wherein, if a next packet is not received even after a predetermined period of time has lapsed since said reception control means receives a packet with a sequence number of transmission indicating that said packet is not the last one among packets consecutively transmitted to said reception control means, said reception-history control means regards said received packet as a last one.

24. A communication control apparatus according to claim 20 wherein, if a packet with a type different from that of a packet received in an immediately preceding reception is received, said reception-history control means regards said packet received in said immediately preceding reception as a last one.

25. A degradation control method for degrading a plurality of synchronized control circuits each provided for a system, said method comprising the steps of:

acquiring information on operating states of said control circuits and information on states of synchronization among said control circuits; and

selecting outputs of two of said control circuits for two corresponding systems provided that said two

control circuits have normal operating states and a normal state of mutual synchronization between said two systems; or

selecting outputs of at least three of said control circuits for at least three corresponding systems provided that said at least three control circuits have normal operating states and normal states of rotational synchronization among said at least three systems.

26. A degradation control method according to claim 25 wherein, in case states of synchronization among all said control circuits are judged to be abnormal, one of said control circuits each with a normal operating state is selected in accordance with a priority order set in advance and said control circuits are operated as a single-system control apparatus based on an output of said selected control circuit.

27. A degradation control method according to claim 25 wherein, with said control circuits operated as a two-system control apparatus,

in case a state of synchronization between two of said control circuits composing said two-system control apparatus are judged to be abnormal, one of said two control circuits each with a normal operating state is selected in accordance with a priority order set in advance and said two control circuits are operated as a single-

system control apparatus based on an output of said selected control circuit; and

in case a state of synchronization between said two control circuits composing said two-system control apparatus are judged to be normal and outputs of said two control circuits each with a normal operating state do not coincide with each other, both control operations of said two control circuits are halted.

28. A synchronous-multisystem control apparatus comprising a plurality of control circuits operating synchronously with each other at a fixed control period to carry out the same processing and an output selector for monitoring operating states of said control circuits and selecting an output of one of said control circuits wherein:

said output selector has a synchronous-multisystem-state storing memory for storing information on operating states of said control circuits and information on states of synchronization among said control circuits and a configuration controller for generating a signal for selecting an output of one of said control circuits; and

said configuration controller generates a signal for selecting an output of one of said control circuits by referring to information stored in said synchronous-multisystem-state storing memory.

29. A synchronous-multisystem control apparatus according to claim 28 wherein said configuration controller selects one of said control circuits each with a normal operating state in accordance with a priority order set in advance and generates a signal for selecting an output of said synchronous-multisystem control apparatus so as to operate said synchronous-multisystem control apparatus as a single-system control apparatus based on said output of said selected control circuit in case all said states of synchronization among said control circuits are judged to be abnormal.

30. A synchronous-multisystem control apparatus according to claim 28 wherein, with said apparatus degraded to a two-system control apparatus,

said configuration controller generates a signal for selecting an output of said synchronous-multisystem such that, in case a state of synchronization between two of said control circuits composing said two-system control apparatus are judged to be abnormal, one of said two control circuits each with a normal operating state is selected in accordance with a priority order set in advance and said two control circuits are operated as a single-system control apparatus based on an output of said selected control circuit; and in case a state of synchronization between said two control circuits composing

said two-system control apparatus are judged to be normal and outputs of said two control circuits each with a normal operating state do not coincide with each other, both control operations of said two control circuits are halted.